Materials Science in Semiconductor Processing 216 (2026) 111099

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Ultrathin sputtered IZO overlayer engineering for high-performance solution-processed oxide TFTs

Changmin An [1], Tae Kyu Nam [1], Hyeon Seok Bae, Sang-Eun Bae, Yo-Han Seo, Dong-Wook Shin [*], Jong Beom Ko [**]

Department of Materials Science and Engineering, Hanbat National University, 125 Dongseo-daero, Yuseong-gu, Daejeon, Republic of Korea

ARTICLE INFO

Keywords:
Solution process
Fabrication process
Oxide thin film transistors
Bilayer
Characteristics modulation

ABSTRACT

We report an IZO bilayer channel architecture for high-performance oxide thin-film transistors (TFTs), where the thickness of the ultrathin sputtered IZO layer on the solution-processed IZO is utilized to control film morphology, carrier transport, and turn-on voltage behavior. A solution-processed IZO bottom layer was fixed at approximately 10 nm, followed by the sputtered IZO overlayer, which was systematically varied from 3 to 5 nm. The addition of the ultrathin sputtered IZO layer significantly improved the electrical properties of the solution-processed IZO TFTs by modulating film morphology and carrier transport behavior. Power-law mobility analysis revealed that the 3 nm bilayer device remains governed by trap-limited conduction, whereas the 4 and 5 nm bilayer devices undergo a gate-field-induced transition from trap-limited conduction to percolation conduction. This transition is attributed to the formation of an interface-assisted percolation pathway around the buried solution IZO/sputtered IZO interface. An optimized 4 nm sputtered IZO overlayer provides the best-balanced performance, including near-zero turn-on voltage, improved switching behavior, mobility enhancement, and gate-voltage controllability, which offers a practical route for high-performance solution-processed oxide TFTs.

1. Introduction

Oxide semiconductor thin-film transistors (TFTs) have emerged as critical components in the development of next-generation large-area electronics, including high-resolution displays, flexible electronics, and transparent devices [1–3]. Among various oxide semiconductors, indium-based oxide materials have attracted considerable attention because of their high carrier mobility, optical transparency, and compatibility with low-temperature fabrication processes [4,5]. In recent years, solution-processed oxide semiconductors have gained increasing interest as a promising alternative to conventional vacuum-deposited oxide films. Solution processing offers several advantages, including low fabrication cost, simple processing steps, and scalability for large-area manufacturing [6]. Despite these benefits, solution-processed oxide TFTs generally show lower electrical performance than vacuum-deposited devices, which is commonly attributed to the relatively limited film quality of solution-derived oxide semiconductors [7].

Various approaches have been explored to improve the electrical performance of solution-processed indium-based oxide TFTs, including precursor chemistry optimization, post-annealing treatments, and interface engineering strategies [8–10]. Recent studies have further highlighted the important roles of carrier-transport mechanisms, interface engineering, and defect-related carrier dynamics in determining the electrical characteristics of metal-oxide TFTs [11–13]. While the strategies can yield partial improvements in device performance, attaining high carrier mobility simultaneously with stable threshold voltage continues to be challenging due to the inherent limitations associated with solution-derived oxide films. A dual active layer architecture combining solution-processed and vacuum-deposited films represents a compelling strategy to leverage the advantages of both techniques while mitigating their respective limitations [14]. However, the fundamental correlation between the thickness of the vacuum-deposited layer and the consequent carrier transport characteristics in these hybrid oxide systems has not been comprehensively elucidated.

In this study, we propose a dual-active-layer oxide TFT architecture

* Corresponding author.
** Corresponding author.
E-mail addresses: dwshin@hanbat.ac.kr (D.-W. Shin), jko914@hanbat.ac.kr (J.B. Ko).
[1] Changmin An[1†] and Tae Kyu Nam[1†] contributed equally to this work and should be considered co-first author.

https://doi.org/10.1016/j.mssp.2026.111099
Received 21 July 2026; Received in revised form 13 August 2026; Accepted 16 August 2026

consisting of a solution-processed indium-zinc-oxide (IZO) bottom layer coupled with an ultrathin sputtered IZO capping layer. The thickness of the sputtered layer was systematically controlled in the ultrathin regime (3–5 nm) to investigate its influence on the electrical performance of IZO TFT. By examining the electrical characterization, surface morphology, and chemical bonding states, we identify a critical sputtering thickness that enables optimal device performance. Our results reveal that the addition of an ultrathin sputtered IZO layer significantly improves the electrical characteristics of solution-processed IZO TFTs, benefitted from altering film morphology and rich chemical bonding states of metal-oxygen. In particular, a sputtered thickness of 4 nm provides the optimal balance between film continuity and carrier concentration, thereby enhancing mobility and exhibiting near-zero turn-on behavior. These findings provide important insight into the design of hybrid oxide semiconductor structures and suggest an effective strategy for improving the performance of low-cost oxide TFT technologies for next-generation display applications.

2. Experimental

For IZO precursor solution, indium nitrate hydrate ($In(NO_3)_3{\cdot}xH_2O$, purity > 99.8%), zinc acetate dihydrate ($Zn(CH_3COO)_2{\cdot}2H_2O$, purity > 98.0%), 2-methoxyethanol, and monoethanolamine (MEA) were purchased from Sigma-Aldrich. To prepare the IZO solution, In and Zn precursor with 0.1 M were prepared in 2-methoxyethanol. The indium and zinc precursor solutions were then combined in a 1:1 vol ratio (corresponding to an In:Zn molar ratio of 5:5). Monoethanolamine (MEA) was added to each solution as a stabilizing agent to suppress premature condensation and improve solution shelf life. The solutions were stirred at 1400 rpm for 1 h at 60 °C to ensure complete dissolution and homogeneous mixing. The final mixed solution was aged at room temperature for more than 12 h prior to use. To remove the undissolved particles from the solution, before use, the solution was filtered through a 0.2 μm polytetrafluoroethylene (PTFE) syringe filter.

Bottom-gate, top-contact structured IZO TFTs were fabricated on heavily doped p-type Si wafers with a thermally grown 100 nm SiO_2 gate dielectric layer, serving as the gate electrode and gate insulator, respectively. The device fabrication processes were carried out using RF/DC sputtering systems (DAON, DaON-1000S), Mask Aligner (PRO WIN, P-150) and wet station system. The fabrication procedures of double layered IZO are illustrated in Fig. 1. The IZO precursor solution was deposited by spin coating at 1500 rpm for 30 s to form the bottom active layer. The coated film was subsequently annealed on a hot plate at 350 °C for 2 h under ambient atmosphere to remove residual organic solvents and promote metal–oxygen bond formation. The sputtered upper IZO layer was deposited by RF magnetron sputtering. The working pressure was maintained at 5 mTorr with an Ar flow rate of 50 sccm, and the RF plasma power was fixed at 350 W. The target thickness of the sputtered layer was set to 3, 4, or 5 nm for the respective device groups. Following dual active layer patterning by photolithography and wet chemical etching, the patterned films underwent a pre-annealing treatment at 200 °C for 1 h to reduce surface roughness and adjust carrier concentration. Source and drain electrodes (100 nm Al) were finally deposited by DC sputtering through a shadow mask, defining a channel width (W) of 1000 μm and a channel length (L) of 600 μm. The morphological characteristics of the IZO layers and electrical properties of the devices were measured using atomic force microscopy (AFM, Park Systems, NX7) and semiconductor device analyzer (B1500A), respectively.

3. Results and discussions

Fig. 2 presents the morphological and structural characterization of the IZO bilayer films as a function of sputtered upper layer thickness. The edge of patterned single and double layer of IZO was measured, and the average thickness of films was collected from their line profiles (Fig. 2(a–c, e–g)). The solution-processed IZO layer had a measured average thickness of approximately 9.68 nm. Average thicknesses of single layer IZO films deposited by sputtering were 2.87 nm, 3.93 nm, and 4.88 nm, respectively, which correspond well with the intended target thickness during sputtering process. The total bilayer thickness reached 10.66, 11.58, and 12.67 nm as the sputtered overlayer thickness increased from 3 to 5 nm (Fig. 2(d)). The thickness contribution of the upper layer was calculated by subtracting the average thickness of the solution-processed base layer (9.68 nm) from the total thickness of the bilayer, showing a consistent reduction of approximately 2 nm from the nominal values across all cases (0.98 nm for 3 nm, 1.90 nm for 4 nm, and 2.99 nm for 5 nm, respectively). It is noteworthy that the initially deposited sputtered IZO partly fills the rough surface valleys of the solution-processed IZO and undergoes nucleation-retarded growth rather than forming a fully continuous layer from the earliest deposition stage (see surface roughness analysis in Fig. 2(h)). The solution-processed single layer exhibits a comparatively elevated surface roughness (Ra) of 1.60 nm, indicative of the particulate surface morphology of solution-processed IZO films. At a target thickness of 3 nm by sputtering, the lowest surface roughness (Ra = 0.55 nm) was observed among all configurations, indicating its suitability for filling the rough surface of solution processed IZO. After a substantial decrease in surface roughness, increasing the target thickness to 5 nm leads to a modest increase in Ra to 1.06 nm, which is still lower than that observed in solution processed IZO. We conclude that the comparatively modest Ra reduction at 3 nm (to 0.55 nm) is consistent with an island-dominated, non-coalesced sputtered film in which isolated nuclei partially cover and smooth the solution surface. As the target thickness increases to 4 nm and beyond, island coalescence is achieved, yielding a laterally continuous dense film.

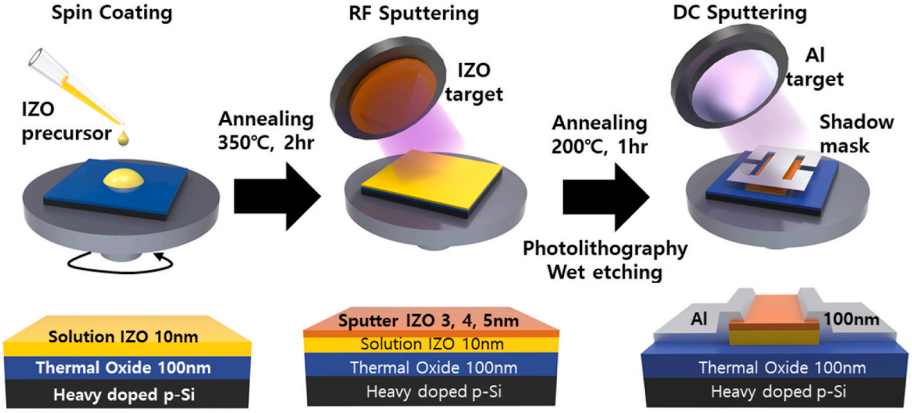

Fig. 1. Schematic illustration of the fabrication process for solution IZO/sputtered IZO bilayer TFTs.

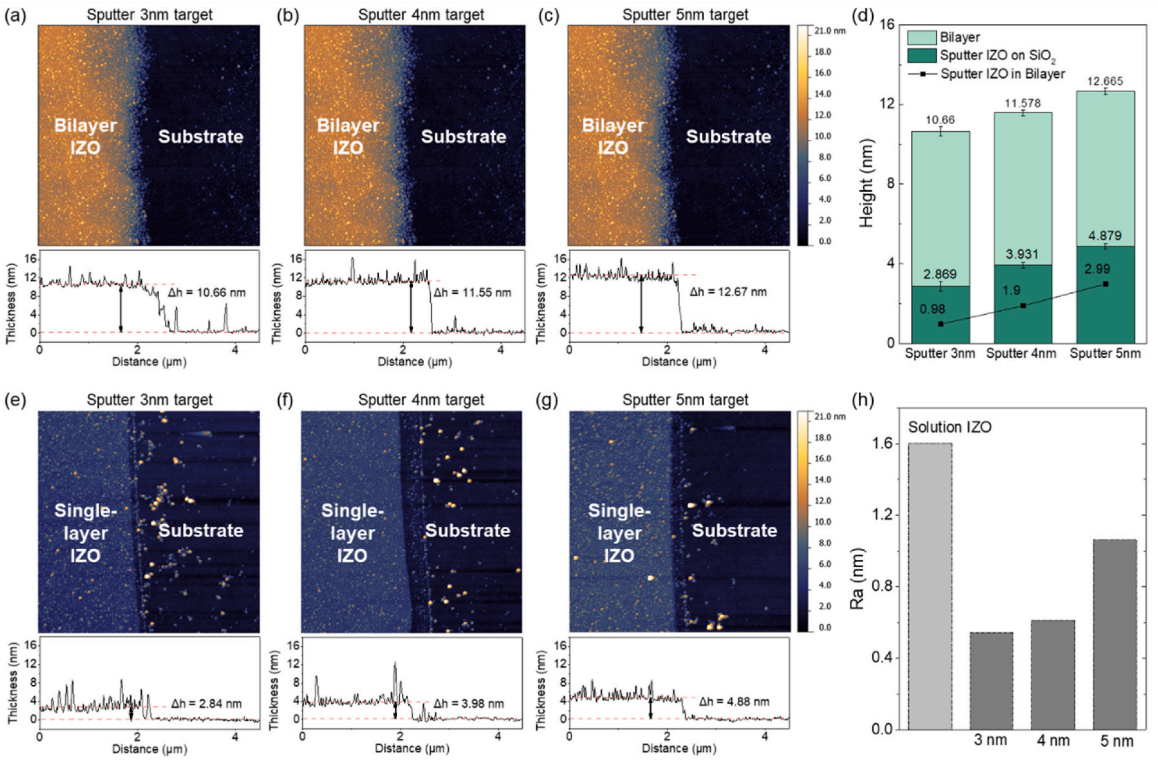

Fig. 2. Morphological and thickness analysis of IZO films with different sputtered IZO thicknesses. AFM height images and line profiles of bilayer IZO films with sputtered IZO thicknesses of (a) 3 nm, (b) 4 nm, and (c) 5 nm. (d) Comparison of bilayer thickness, sputtered IZO thickness on SiO_2, and estimated sputtered IZO contribution in the bilayer. AFM height images and line profiles of single-layer sputtered IZO films with thicknesses of (e) 3 nm, (f) 4 nm, and (g) 5 nm. (h) Surface roughness of solution IZO and bilayer IZO films.

Fig. 3(a) shows the transfer characteristics of the IZO TFTs at $V_D = 0.1$ V across all four fabrication conditions (solution single-layer, bilayer with 3 nm, 4 nm, and 5 nm sputter layer). Fig. 3(b) and Table S1 summarize the extracted device parameters averaged devices per condition. Individual device transfer curves from the solution single-layer and all three bilayers are provided in Fig. S1, demonstrating the reproducibility of each device group. The solution single-layer device exhibits poorly defined switching behavior with a very low drain current level, consistent with a high density of trap states and deficient carrier transport in the defect-rich solution-processed film. The bilayer device with a 3 nm sputtered overlayer shows marginal enhancement in on/off switching; however, it continues to exhibit a low ON current and large subthreshold-swing (S.S). This behavior is attributed to the incomplete coalescence of the sputtered film at this thickness, resulting in the channel being predominantly influenced by the defect-rich solution layer [6].

In contrast, the bilayer devices with 4 nm and 5 nm sputtered layers demonstrate clearly improved transfer characteristics with significantly increased mobility values and decreased S.S. The abrupt decrease in S.S. from 4.16 V dec^{-1} for the 3 nm bilayer device to approximately 0.90–0.92 V dec^{-1} for the 4 and 5 nm bilayer devices suggests that the effective trap contribution involved in subthreshold transport is substantially reduced once the sputtered IZO overlayer reaches a critical thickness. This improvement may not be fully explained by changes at the gate-insulator/solution-IZO interface alone. Instead, it may reflect an evolution of carrier transport in the bilayer channel, including possible changes in the effective conducting path near the solution IZO/sputtered IZO interfacial region. Among the bilayer devices, the 4 nm device presents the most balanced performance profile with reasonable turn-on voltage (V_{on}) and field-effect mobility (μ_{FE}) of −0.30 V and 13.80 $cm^2V^{-1}s^{-1}$, respectively. V_{on} was extracted as the gate voltage at which the normalized drain current ($I_D \times L/W$) reached 1 nA. The device with 5 nm layer achieves a higher mobility but exhibits a pronounced negative shift in V_{on} compared with the 4 nm device. The output characteristics of the most balanced device (4 nm bilayer) show well-defined linear and saturation regions with clear current saturation at high drain voltages, confirming ideal TFT operation (Fig. S2).

To gain deeper insight into the carrier transport mechanisms governing the bilayer TFTs, we employed the empirical power-law model, which has been effectively used in previous bilayer and heterostructure oxide TFT studies to comparatively evaluate gate-field-dependent carrier transport behavior [15–17]:

$$\mu_{FE} = K(V_G - V_{T,P})^{\gamma}$$

where V_T and V_P are the threshold and percolation voltage, respectively, and the prefactor K and exponent γ are associated with the intrinsic carrier transport characteristics. In particular, γ provides information on the dominant charge transport mechanism in oxide semiconductor TFTs. A γ value close to 0.7 is indicative of trap-limited conduction (TLC), where carrier transport is primarily governed by localized tail states and trap filling. In contrast, a significantly lower γ value, approaching 0.1, denotes percolation conduction (PC), where carriers move through spatially connected potential pathways after a substantial fraction of trap states has been filled. The prefactor K also provides useful information on trap-related transport. In the TLC regime, a higher K value indicates reduced interference from electron traps during electron conduction [16,17]. Each bilayer TFT with a 3, 4 and 5 nm sputtered IZO layer was separately examined in the low- and high-gate field regime, as indicated in Fig. 4(a). The overlapped μ_{FE}—V_G curves for all devices are summarized in Fig. S3. For the device with a 3 nm sputtered IZO layer, the power-law model fits the mobility behavior over a broad V_G range with a γ value of approximately 0.72 and a very small K value of 0.05. Even after covering with a 3 nm sputtered overlayer, TLC-dominated transport still occurs due to the high density of trap states and deficient carrier transport in the defect-rich solution-processed film, causing

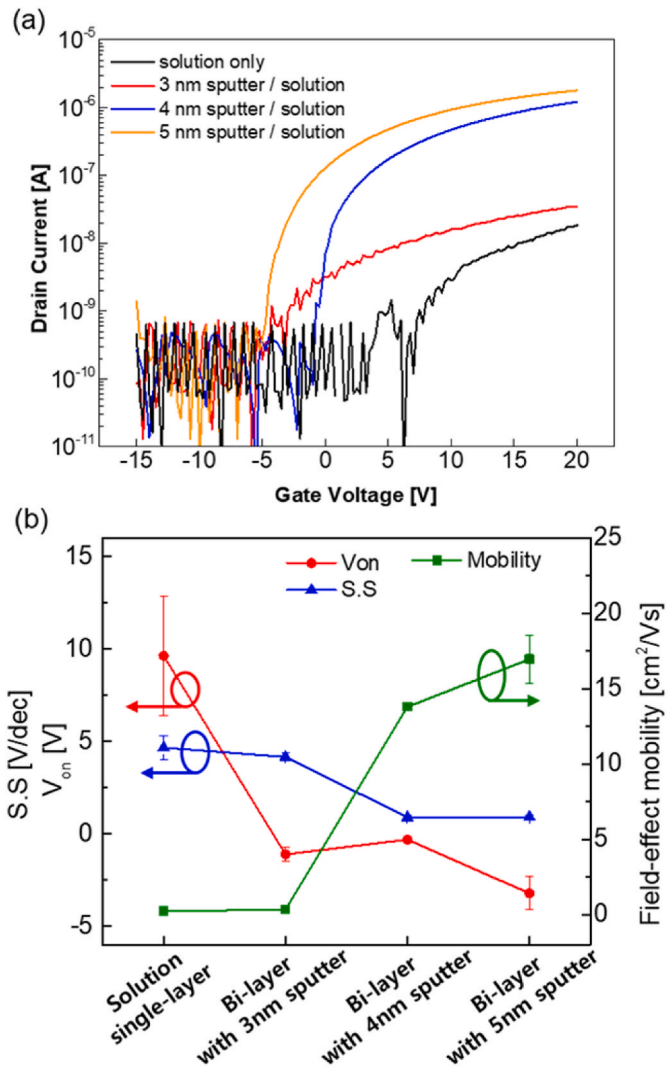

Fig. 3. Electrical characteristics of solution IZO and solution IZO/sputtered IZO bilayer TFTs. (a) Transfer characteristics measured at $V_D = 0.1$ V. (b) Extracted device parameters as a function of sputtered IZO thickness.

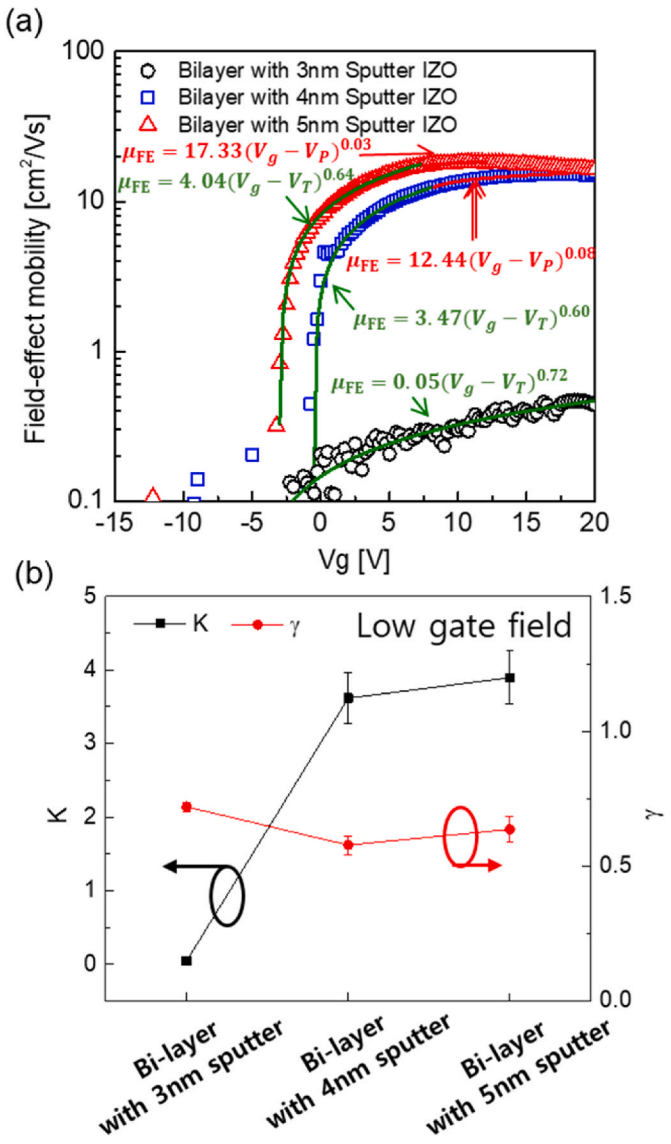

Fig. 4. Gate-field-dependent carrier transport analysis of bilayer IZO TFTs. (a) Field-effect mobility as a function of gate voltage fitted using the power-law model. (b) Extracted K and γ values in the low-gate-field.

current path confinement at the gate insulator/IZO interface. This is attributed to the insufficient thickness of the 3 nm sputtered layer, which is inadequate to form a continuous conductive network and the current path remains predominantly governed by the trap-rich bottom solution IZO channel.

In contrast, the bilayer TFTs with 4 and 5 nm sputtered IZO layers exhibit two distinguishable transport regimes. In the low-gate field regime, the extracted γ values remain relatively high and comparable, with exhibiting values of approximately 0.60 and 0.64 for the 4 and 5 nm bilayer devices, respectively. This suggests that TLC still dominates during the early stage of channel formation. However, the corresponding *K* values increase dramatically to 3.47 and 4.04, respectively, which are approximately 70-80 times larger than that of the 3 nm bilayer device as depicted in Fig. 4(b). This pronounced increase in *K* suggests that the trap-limited transport is substantially relieved once the sputtered IZO overlayer reaches sufficient continuity. Together with the abrupt improvement in S.S., this result implies that the effective carrier transport environment is no longer governed solely by the trap-rich solution IZO region, but becomes increasingly influenced by the solution IZO/sputtered IZO interfacial region. In the high-gate field regime, the transport behavior of the 4 and 5 nm bilayer TFTs changes markedly. The γ values decrease substantially to 0.08 and 0.03 for the 4 and 5 nm sputtered IZO devices, respectively, indicating a transition from TLC-dominated transport to PC-dominated transport. This transition can be understood as a consequence of progressive trap filling below the conduction band minimum and the formation of spatially connected percolation pathways.

Importantly, the enhanced mobility of the bilayer TFTs cannot be attributed simply to direct conduction through the sputtered IZO layer itself. As shown in Fig. S4, the single-layer sputtered IZO TFTs with thicknesses of 4 and 5 nm IZO exhibit much lower field-effect mobilities of approximately 0.1 and 3 $cm^2V^{-1}s^{-1}$, respectively, compared with the corresponding bilayer TFTs showing mobilities exceeding 13 $cm^2V^{-1}s^{-1}$. We emphasize that the ultrathin sputtered IZO layer alone does not serve as the primary efficient conducting channel. Therefore, the mobility enhancement in the bilayer TFTs should be understood in terms of an interfacial transport, which is driven by the synergistic coupling between the bottom solution-processed IZO and the top sputtered IZO layer.

The difference between the 4 and 5 nm devices is particularly important. In both devices, the reduced γ values in the high-gate-field regime indicate a transition from TLC-dominated transport to PC-like transport, suggesting that an interface-assisted carrier pathway is

formed near the solution IZO/sputtered IZO interface. However, their turn-on characteristics are markedly different. The 4 nm device exhibits a near-zero V_{on} while maintaining improved mobility, indicating that the optimized thickness of sputtered IZO overlayer effectively promotes interfacial transport while limiting excess carrier accumulation. In contrast, the 5 nm bilayer TFT shows a significant negative V_{on} shift, suggesting excessive carrier accumulation induced by the thicker sputtered IZO overlayer. This behavior is consistent with the greater carrier contribution of the thicker sputtered IZO layer, as supported by the single-layer control devices (Fig. S4): the 5 nm single-layer TFT exhibits both a higher current level and a more negative V_{on} than the 4 nm counterpart. When incorporated into the bilayer structure, this greater carrier contribution from the 5 nm sputtered IZO promotes carrier accumulation at the solution IZO/sputtered IZO interface, driving the negative V_{on} shift and weakening gate electrostatic control. Therefore, the optimized transport in the bilayer TFTs is not governed by the sputtered IZO layer as a standalone conducting channel, but by the formation of an interface-assisted percolation pathway at the solution IZO/sputtered IZO interface. From this viewpoint, the 4 nm sputtered IZO overlayer provides the most balanced configuration, enabling the transition from TLC to PC while suppressing excessive carrier accumulation and preserving gate voltage controllability. Although the present electrical analysis does not directly identify the spatial conduction pathway, the consistent variations in the power-law parameters, S.S., and electrical characteristics of the single-layer control devices collectively support the proposed interface-assisted transport interpretation.

To further investigate the chemical bonding states of the IZO films, XPS was performed on the O 1s core-level spectra for all fabrication conditions. The O 1s spectra were deconvoluted into three sub-peaks: the lattice oxygen (M − O) bonding component at the lowest binding energy (~530 eV), the oxygen-deficient related component (V_O) at an intermediate binding energy (~531 eV), and the chemisorbed hydroxyl and organic species (OH/OC) at the highest binding energy (~532 eV) [18,19]. The relative fraction of each component as a function of the film fabrication condition is summarized in Fig. 5(c). For the solution single-layer IZO film (Fig. 5(a)), the O 1s spectrum is dominated by the OH/OC component (0.56), with a substantial V_O fraction (0.33) and a minor M − O contribution (0.10). The large OH/OC fraction is consistent with the nature of solution-processed oxide films, which can retain residual hydroxyl groups and organic ligands from the sol-gel precursor even after thermal annealing. In addition, the relatively high V_O and OH/OC fraction indicate a chemically disordered and trap-rich oxide network, providing a plausible origin for trap-limited carrier transport when the current path is mainly confined to the solution IZO region. In contrast, the 20 nm sputtered IZO single-layer reference (Fig. 5(b)) shows a substantially higher M − O fraction (0.65) and lower OH/OC content (0.14), consistent with the relatively well-coordinated nature of sputter-deposited oxide films compared with solution-processed films. This clear chemical contrast between the solution-processed and sputter-deposited IZO is qualitatively consistent with the transport evolution discussed in the preceding power-law mobility analysis, where the contribution of trap-limited transport is substantially reduced upon sufficient development of the sputtered IZO overlayer. The O 1s spectra of the bilayer films are provided in Fig. S5 for completeness; however, owing to the surface-sensitive nature of XPS and the increasing contribution of the sputtered overlayer with increasing thickness, these spectra were not used to interpret the chemical state of the buried solution IZO/sputtered IZO interface.

Fig. 6 benchmarks the relationship between V_{on} and mobility for reported solution-processed In-Zn-O based TFTs [11,20–26]. Compared with previously reported solution-processed In-Zn-O based TFTs, the optimized solution/sputter IZO TFT exhibits competitive mobility while maintaining a near-zero V_{on}. This result highlights that ultrathin sputtered IZO overlayer engineering provides an effective route to balance carrier transport enhancement and gate-voltage controllability.

4. Conclusions

We developed a solution IZO/sputtered IZO bilayer TFT architecture where the ultrathin sputtered IZO overlayer thickness dictates film morphology, interfacial carrier transport, and turn-on behavior. Line profiles of the patterned IZO films in AFM analysis revealed nucleation-

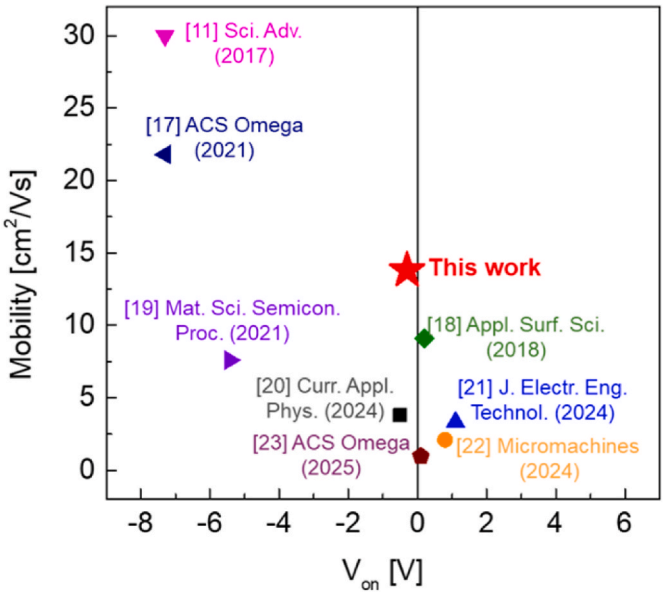

Fig. 6. Benchmarking of mobility versus V_{on} for reported solution-processed In–Zn–O-based TFTs [11,20–26].

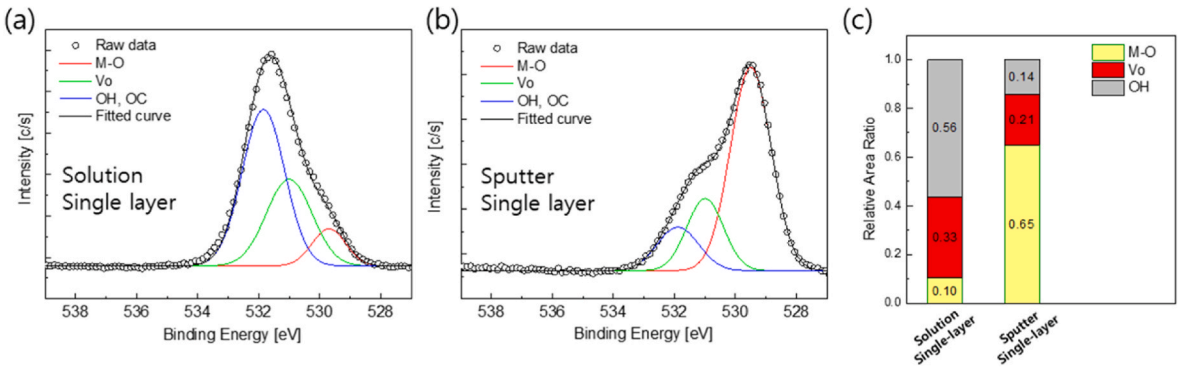

Fig. 5. XPS O 1s spectra of IZO films with different channel structures. Deconvoluted O 1s spectra of (a) solution IZO, and (b) single-layer sputtered IZO. (c) Relative fractions of M − O, V_O, and OH/OC components extracted from the O 1s spectra.

retarded growth of sputtered IZO on the solution-processed IZO surface, resulting in the actual thickness below the nominal target. The overlayer reduced the surface roughness of the underlying film, with a nominal 4 nm thickness providing the most balanced morphology and device characteristics. Consequently, bilayer TFT with 4 nm overlayer delivered the finest balance between mobility improvement and V_{on} controllability. Power-law mobility analysis revealed field induced transition from TLC-dominated (low gate fields) to PC-dominated transport (high gate fields), signifying an interface-assisted percolation pathway near the solution IZO/sputtered IZO interface. In contrast, the bilayer with 5 nm overlayer suffered from excessive carrier accumulation and a negative V_{on} shift despite its superior PC metrics (larger K value and smaller γ value), resulting in weakened gate control. XPS O 1s analysis further revealed distinct chemical characteristics between the solution-processed and sputter-deposited IZO, with the sputtered IZO reference exhibiting a higher M − O fraction and lower OH/OC content. This chemical contrast is qualitatively consistent with the reduced contribution of trap-limited transport observed in the power-law mobility analysis. Together, these insights support that the optimized performance of the 4 nm bilayer TFT stems from a balanced interface-assisted percolation pathway that boosts carrier transport while preserving bottom-gate electrostatic control.

CRediT authorship contribution statement

Changmin An: Conceptualization, Formal analysis, Investigation, Validation. **Tae Kyu Nam:** Visualization, Writing – original draft. **Hyeon Seok Bae:** Investigation. **Sang-Eun Bae:** Formal analysis. **Yo-Han Seo:** Investigation. **Dong-Wook Shin:** Conceptualization, Resources, Supervision, Writing – review & editing. **Jong Beom Ko:** Conceptualization, Resources, Supervision, Writing – original draft.

Declaration of competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This work was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education (RS-2023-00250816). This research was also supported by the ANCHOR program through the Daejeon ANCHOR Center, funded by the Ministry of Education (MOE) and the Daejeon Metropolitan City, Republic of Korea (2026-ANCHOR-06-002).

Device fabrication and characterization were performed at the Semiconductor Fabrication Center of Hanbat National University using RF/DC sputtering, mask aligner, wet-station, and AFM facilities.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mssp.2026.111099.

Data availability

Data will be made available on request.

References

[1] H.-H. Hsieh, H.-H. Lu, H.C. Ting, C.-S. Chuang, C.-Y. Chen, Y. Lin, Development of IGZO TFTs and their applications to next-generation flat-panel displays, J. Infect. Dis. 11 (2010) 160–164.

[2] T.Z. Wu, C.W. Sher, Y. Lin, C.-F. Lee, S.J. Liang, Y.J. Lu, S.W.H. Chen, W.J. Guo, H.-C. Kuo, Z. Chen, Mini-LED and micro-LED: promising candidates for the next generation display technology, Appl. Sci. 8 (2018) 1557, https://doi.org/10.3390/app8091557.

[3] J.B. Ko, S.H. Lee, K.W. Park, S.K. Park, Interface tailoring through the supply of optimized oxygen and hydrogen to semiconductors for highly stable top-gate-structured high-mobility oxide thin-film transistors, RSC Adv. 9 (2019) 36293–36300.

[4] T. Kamiya, K. Nomura, H. Hosono, Present status of amorphous In–Ga–Zn–O thin-film transistors, Sci. Technol. Adv. Mater. 11 (2010) 044305, https://doi.org/10.1088/1468-6996/11/4/044305.

[5] T. Kamiya, H. Hosono, Material characteristics and applications of transparent amorphous oxide semiconductors, NPG Asia Mater. 2 (2010) 15–22, https://doi.org/10.1038/asiamat.2010.5.

[6] S.R. Thomas, P. Pattanasattayavong, T.D. Anthopoulos, Solution-processable metal oxide semiconductors for thin-film transistor applications, Chem. Soc. Rev. 42 (2013) 6910–6923, https://doi.org/10.1039/C3CS35402D.

[7] J.W. Park, B.H. Kang, H.J. Kim, A review of low-temperature solution-processed metal oxide thin-film transistors for flexible electronics, Adv. Funct. Mater. 30 (2020) 1904632.

[8] H.C. You, Transistor characteristics of zinc oxide active layers at various zinc acetate dihydrate solution concentrations of zinc oxide thin-film, J. Appl. Res. Technol. 13 (2015) 291–296, https://doi.org/10.1016/j.jart.2015.06.003.

[9] B.S. Yu, J.Y. Jeon, B.C. Kang, W. Lee, Y.-H. Kim, T.-J. Ha, Wearable 1 V operating thin-film transistors with solution-processed metal-oxide semiconductor and dielectric films fabricated by deep ultra-violet photo annealing at low temperature, Sci. Rep. 9 (2019) 8416, https://doi.org/10.1038/s41598-019-44948-z.

[10] W. Lee, J. Kim, Y.-H. Kim, High-performance InOx/GaOx bilayer channel thin-film transistors made using persistent high-surface-energy induced by photochemical activation, J. Alloys Compd. 723 (2017) 627–632.

[11] H.U. Huzaibi, S.-T. Han, M. Zhang, Model representation in amorphous metal oxide thin-film transistors: a critical review, npj Flexible Electron. 10 (2026) 13.

[12] B. Wang, X. Xu, F. Chen, Y. Yan, Y. Zhou, S. Han, M. Zhang, Performance enhancement of indium gallium zinc oxide thin-film transistors through optimization of the octadecylphosphonic acid self-assembled monolayer process, Surf. Interfaces 85 (2026) 108677.

[13] M. Zhang, B. Wang, Y. Zhao, Z. Jiang, L. Lu, Y. Yan, L.-C. Chen, M. Wong, H.-S. Kwok, Low frequency noise of elevated-metal metal-oxide thin-film transistor, IEEE Electron Device Lett. 46 (2025) 432–435.

[14] H. Faber, S. Das, Y.-H. Lin, N. Pliatsikas, K. Zhao, T. Kehagias, G. Dimitrakopulos, A. Amassian, P.A. Patsalas, T.D. Anthopoulos, Heterojunction oxide thin-film transistors with unprecedented electron mobility grown from solution, Sci. Adv. 3 (2017) e1602640, https://doi.org/10.1126/sciadv.1602640.

[15] J. Krausmann, S. Sanctis, J. Engstler, M. Luysberg, M. Bruns, J.J. Schneider, Charge transport in low-temperature processed thin-film transistors based on indium oxide/zinc oxide heterostructures, ACS Appl. Mater. Interfaces 10 (2018) 20661–20671.

[16] F. He, Y. Qin, L. Wan, J. Su, Z. Lin, J. Zhang, J. Chang, J. Wu, Y. Hao, Metal oxide heterojunctions for high performance solution grown oxide thin film transistors, Appl. Surf. Sci. 527 (2020) 146774.

[17] J. Lee, J.-S. Eun, J.-H. Na, W. Park, J.-H. Park, J. Feng, J. Jang, I.M. Kang, J. Park, X. Zhang, D.-K. Kim, J.-H. Bae, Verifying the physical role of upper-active-layer on charge transport together with bias stability in bilayer-channel oxide thin-film transistors, Surf. Interfaces 51 (2024) 104624.

[18] J.B. Ko, S.-I. Cho, S.-H.K. Park, Engineering a subnanometer interface tailoring layer for precise hydrogen incorporation and defect passivation for high-end oxide thin-film transistors, ACS Appl. Mater. Interfaces 15 (2023) 47799–47809.

[19] S. Jeong, J.Y. Lee, S.S. Lee, Y.H. Seo, S.Y. Kim, J.U. Park, B.H. Ryu, W. Yang, J. Moon, Y. Choi, Metal salt-derived In-Ga-Zn-O semiconductors incorporating formamide as a novel co-solvent for producing solution-processed, electrohydrodynamic-jet printed, high-performance oxide transistors, J. Mater. Chem. C 1 (2013) 4236–4243, https://doi.org/10.1039/c3tc30530a.

[20] A.M. Weidling, V.S. Turkani, B. Luo, K.A. Schroder, S.L. Swisher, Photonic curing of solution-processed oxide semiconductors with efficient gate absorbers and minimal substrate heating for high-performance thin-film transistors, ACS Omega 6 (2021) 17323–17334.

[21] W. Xu, L. Hu, C. Zhao, L. Zhang, D. Zhu, P. Cao, W. Liu, S. Han, X. Liu, F. Jia, Y. Zeng, Y. Lu, Low temperature solution-processed IGZO thin-film transistors, Appl. Surf. Sci. 455 (2018) 554–560.

[22] A.S. Safaruddin, J.P.S. Bermundo, M.P.A. Jallorina, A. Yamamoto, Y. Uraoka, Spray pyrolyzed fluorinated inorganic-organic passivation for solution-processed a-InZnO thin-film transistors, Mater. Sci. Semicond. Process. 146 (2022) 106669.

[23] X. Zhang, N.N. Mude, S.W. Cho, Enhanced electrical performance and stability of solution-processed oxide semiconductor thin-film transistors via an incorporation of deionized water oxidizer, Curr. Appl. Phys. 68 (2024) 78–84.

[24] S. You, A. Tukhtaev, G. Tarsoly, H.L. Zhao, X.L. Wang, F. Shan, J.-Y. Lee, J.H. Lee, S.I. Jang, Y.J. Jeong, S.-J. Kim, Electrical characteristics of multi-layered, solution-processed indium zinc oxide thin-film transistors, J. Electr. Eng. Technol. 19 (2024) 2521–2526, https://doi.org/10.1007/s42835-023-01689-4.

[25] X. Zhang, S.-W. Cho, Solution process-based thickness engineering of InZnO semiconductors for oxide thin-film transistors with high performance and stability, Micromachines 15 (2024) 193, https://doi.org/10.3390/mi15020193.

[26] N.M. Thazin, J.P.S. Bermundo, U. Hanifah, J. Richter, S. Geburt, Y. Uraoka, Solid-state laser annealing (SLA) of fully solution-processed amorphous InZnO thin-film transistors at various fluence, ACS Omega 10 (2025) 14001–14009.